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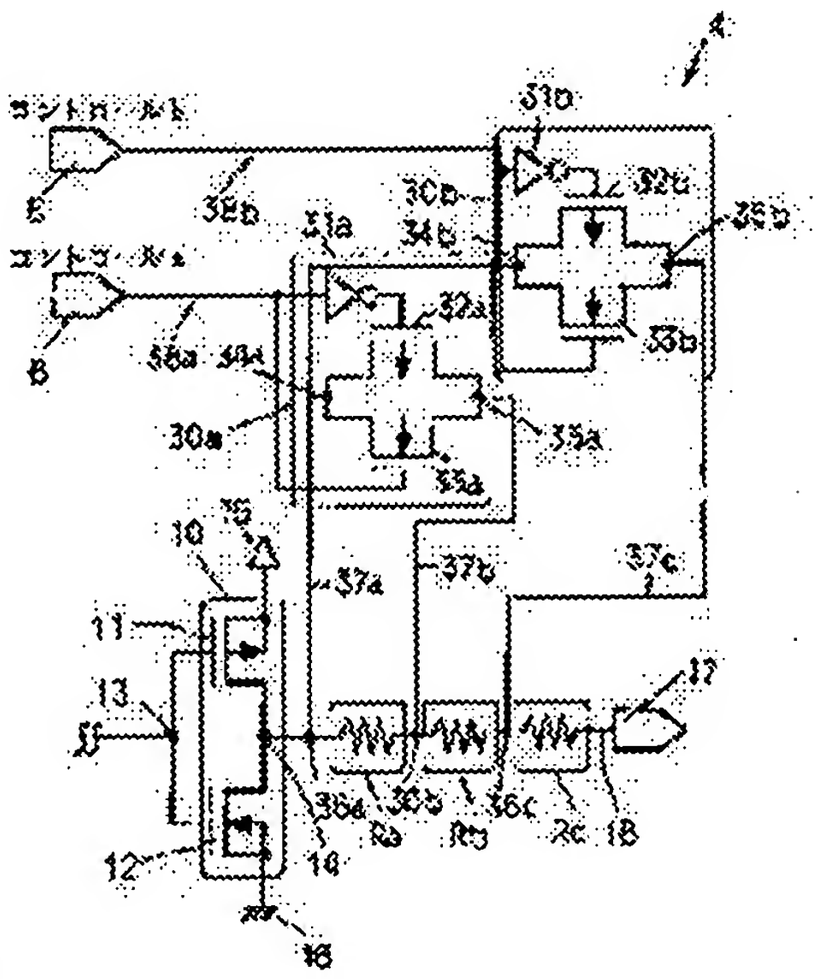
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ELECTRONIC DEVICE, AND MANUFACTURE OF THE ELECTRONIC DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To enable the selective and adjustable use of an output impedance by providing control terminals for changing over resistance values connected to each switch circuit, to which signals are inputted for controlling the switch circuits.

SOLUTION: When the LOW signal is inputted to control terminal controls (a),(b) for changing over the resistnace vlaue, the resistance value of the output part becomes the total of the resistance values of resistors Ra-Rc. When the HIGH signal is inputted to the control terminal control (a) for changing over the resistance value and the LOW signal is inputted to the control terminal control (b) for changing over the resistance value, the resistance value of the output part becomes the total of the resistance values of the resistors Rb, Rc. Also, when the HIGH signal is inputted to the control (b), the resistance value becomes that of the resistor Rc only. The switch circuits 30a, 30b are operated by the voltage applied on the controls (a), (b), and the different current route is formed between an output node 14 and an output terminal 17, thereby the output impedance of a driver IC 4 is selected and adjusted.



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CLAIMS

[Claim(s)]
[Claim 1] In order to adjust an output impedance between an output stage driver component, an output terminal, the 1st reference potential terminal (power supply terminal), or the 2nd reference potential terminal (grand terminal), two or more resistance and two or more switching circuits are prepared. The resistance change circuit which has two or more current paths in which resistance changes mutually with combination of said resistance and switching circuit between said output stage driver component and said output terminal, said 1st reference potential terminal, or said 2nd reference potential terminal is constituted. Semiconductor integrated circuit equipment characterized by preparing the control terminal for a resistance change into which the signal which is connected to said each switching circuit and controls a switching circuit is inputted.
[Claim 2] Said control terminal for a resistance change is semiconductor integrated circuit equipment according to claim 1 characterized by being the terminal with which the 1st reference potential (power-source potential) or the 2nd reference potential (ground potential) is impressed.
[Claim 3] Said semiconductor integrated circuit equipment is semiconductor integrated circuit equipment according to claim 1 or 2 characterized by constituting the driver IC.
[Claim 4] In order to be carried in a mounting substrate and said mounting substrate and to adjust an output impedance between an output stage driver component, an output terminal, the 1st reference potential terminal (power supply terminal), or the 2nd reference potential terminal (grand terminal), two or more resistance and two or more switching circuits are prepared. The resistance change circuit which has two or more current paths in which resistance changes mutually with combination of said resistance and switching circuit between said output stage driver component and said output terminal, said 1st reference potential terminal, or said 2nd reference potential terminal is constituted. The 1st semiconductor integrated circuit equipment with which it comes to prepare the control terminal for a resistance change into which the signal which is connected to said each switching circuit, and controls a switching circuit is inputted, It has the 2nd semiconductor integrated circuit equipment electrically connected to said 1st semiconductor integrated circuit equipment through wiring of said mounting substrate. Said control terminal for a resistance change is an electronic instrument characterized by connecting with either the 1st reference potential wiring (power-source wiring) of said mounting substrate or the 2nd reference potential wiring (grand wiring).
[Claim 5] Said 1st semiconductor integrated circuit equipment is an electronic instrument according to claim 4 characterized by constituting the driver IC.
[Claim 6] It is the electronic instrument according to claim 4 or 5 which said 1st semiconductor integrated circuit equipment is a driver IC, and said 2nd semiconductor integrated circuit equipment is Memory IC, and is characterized by constituting the memory module on the whole.
[Claim 7] In order to adjust an output impedance between a mounting substrate, and an output stage driver component, an output terminal, the 1st reference potential terminal (power supply terminal) or the 2nd reference potential terminal (grand terminal), two or more resistance and two or more switching circuits are prepared. The resistance change circuit which has two or more current paths in which

resistance changes mutually with combination of said resistance and switching circuit between said output stage driver component and said output terminal, said 1st reference potential terminal, or said 2nd reference potential terminal is constituted. The 1st semiconductor integrated circuit equipment with which it comes to prepare the control terminal for a resistance change into which the signal which is connected to said each switching circuit, and controls a switching circuit is inputted, The process which prepares two or more 2nd semiconductor integrated circuit equipments electrically connected to said 1st semiconductor integrated circuit equipment through wiring of said mounting substrate, The process which carries said 1st semiconductor integrated circuit equipment and the 2nd semiconductor integrated circuit equipment in said mounting substrate, It judges based on the property of said mounting substrate or the 2nd semiconductor integrated circuit equipment. The control terminal for a resistance change of said 1st semiconductor integrated circuit equipment to the 1st reference potential wiring (power-source wiring) or the 2nd reference potential wiring (grand wiring) of said mounting substrate by the electrical connecting means The manufacture approach of the electronic instrument characterized by having the process to connect.

[Claim 8] It is the manufacture approach of the electronic instrument according to claim 7 which prepares branching wiring for performing electrical installation with said control terminal for a resistance change in the 1st reference potential wiring (power-source wiring) or the 2nd reference potential wiring (grand wiring) of said mounting substrate, and is characterized by connecting said control terminal for a resistance change to said one of branching wiring electrically.

[Claim 9] It is the manufacture approach of the electronic instrument according to claim 7 or 8 which said 1st semiconductor integrated circuit equipment is a driver IC, and said 2nd semiconductor integrated circuit equipment is Memory IC, and is characterized by constituting the memory module on the whole.

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TECHNICAL FIELD

[Field of the Invention] Especially this invention applies to the technique aim at adjustment with the output impedance of semiconductor integrated circuit equipments, such as a driver IC, and the input impedance of other semiconductor integrated circuit equipments which consist of memory IC connected to said semiconductor integrated circuit equipment, and adjustment with the wiring impedance connected to said semiconductor integrated circuit equipment, and aim at delivery of the stable signal, with respect to semiconductor integrated circuit equipment (semiconductor device), an electronic instrument, and the manufacture approach of the electronic instrument, and relates to an effective technique.

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EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
(1) Selection adjustment of the output impedance of a driver IC can be attained.
(2) In a memory module, since a driver IC can perform selection adjustment of an output impedance, it can perform adjustment with the input impedance of Memory IC, and a wiring impedance. Consequently, distortion of the output wave of a driver IC stops occurring, and the signal between a driver IC and Memory IC can be delivered good.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As a memory module 1 is shown in drawing 7 , two or more memory IC 3 and driver ICs 4 are carried in the mounting substrate (board: memory module substrate) 2. While wiring 5 is formed in the board 2, a terminal 6 is located in a line and prepared in one side of a board 2. Memory IC 3 and the external terminal of a driver IC 4 are connected to the predetermined wiring 5, respectively.
[0007] Although said terminal 6 does not carry out especially illustration, it consists of the 1st reference potential terminal (power supply terminal: Vcc), the 2nd reference potential terminal (gland: GND), a clock terminal (CLK), an input terminal, an output terminal, and various kinds of control terminals.
[0008] Drawing 8 is the example which formed resistance 19 in the wiring 18 which shows an example of the output stage circuit of the conventional driver IC 4, and connects electrically the output node 14 and output terminal 17 of the output stage driver component 10 of an output stage circuit. Said output stage driver component 10 is a CMOS inverter circuit which consists of N-channel metal oxide semiconductor FET11 and P channel MOSFET12.
[0009] Although the output terminal 17 of such an output stage circuit is connected to the predetermined terminal of memory IC 3 through the wiring 5 of the memory module substrate 2, when neither the impedance of wiring 5 nor the impedance of memory IC 3 is in agreement, as shown in the wave form chart of drawing 9 , turbulence occurs in a wave. the wave which reflection does not generate by the impedance matching at the time of drawing 9 setting a time-axis (T) as an axis of abscissa A, and making an axis of ordinate B into an electrical potential difference (V) and which should be expected -- 20 and the wave which distortion generated by the impedance mismatch -- 21 is shown.
[0010] It is effective by the case where the input impedance of the memory IC which connects with the wiring impedance of the board carried that the impedance by the output stage driver component of a driver IC and resistance doubles like before (adjustment) is always the same. Therefore, when the quality of the material and the wire length of the board carried differ from each other, or when driving the memory IC from which an input impedance differs, it becomes the inequality (mismatching) of an impedance, and distortion arises in the output wave of a driver IC, and the connected memory IC malfunctions.
[0011] Although this malfunction is solvable by adjusting the resistance of an output stage circuit and doubling the impedance of an output stage, for a double lump, modification of the photo mask used at the last process in the process which manufactures a driver IC is needed, and there are many demerits of chip makers or a board manufacturer.
[0012] The purpose of this invention is to offer the semiconductor integrated circuit equipment (driver IC) in which selection adjustment use of an output impedance is possible.
[0013] Other purposes of this invention are in the electronic instrument which has the semiconductor integrated circuit equipment which has an output stage circuit, and other semiconductor integrated circuit equipments connected to this semiconductor integrated circuit equipment to offer the electronic instrument which can attain delivery of a good signal, and its manufacture approach, without making the output wave of said output stage circuit generate distortion.

[0014] Other purposes of this invention are to offer the memory module which can be performed by a good signal delivering, without making an output wave generate distortion.
[0015] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.

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MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
(1) In order to adjust an output impedance between an output stage driver component, an output terminal, the 1st reference potential terminal (power supply terminal), or the 2nd reference potential terminal (grand terminal), two or more resistance and two or more switching circuits are prepared. The resistance change circuit which has two or more current paths in which resistance changes mutually with combination of said resistance and switching circuit between said output stage driver component and said output terminal, said 1st reference potential terminal, or said 2nd reference potential terminal is constituted. Semiconductor integrated circuit equipment with which it comes to prepare the control terminal for a resistance change into which the signal which is connected to said each switching circuit and controls a switching circuit is inputted. Said control terminal for a resistance change is a terminal with which the 1st reference potential (power-source potential) or the 2nd reference potential (ground potential) is impressed. Said semiconductor integrated circuit equipment constitutes the driver IC.
[0017] (2) In order to be carried in a mounting substrate and said mounting substrate and to adjust an output impedance between an output stage driver component, an output terminal, the 1st reference potential terminal (power supply terminal), or the 2nd reference potential terminal (grand terminal), two or more resistance and two or more switching circuits are prepared. The resistance change circuit which has two or more current paths in which resistance changes mutually with combination of said resistance and switching circuit between said output stage driver component and said output terminal, said 1st reference potential terminal, or said 2nd reference potential terminal is constituted. The 1st semiconductor integrated circuit equipment with which it comes to prepare the control terminal for a resistance change into which the signal which is connected to said each switching circuit, and controls a switching circuit is inputted, It has the 2nd semiconductor integrated circuit equipment electrically connected to said 1st semiconductor integrated circuit equipment through wiring of said mounting substrate. Said control terminal for a resistance change is an electronic instrument which it comes to connect to either the 1st reference potential wiring (power-source wiring) of said mounting substrate or the 2nd reference potential wiring (grand wiring). Said 1st semiconductor integrated circuit equipment constitutes the driver IC. Said 1st semiconductor integrated circuit equipment is a driver IC, and said 2nd semiconductor integrated circuit equipment is Memory IC, and constitutes the memory module on the whole.
[0018] Such an electronic instrument is manufactured by the following manufacture approaches. In order to adjust an output impedance between a mounting substrate, and an output stage driver component, an output terminal, the 1st reference potential terminal (power supply terminal) or the 2nd reference potential terminal (grand terminal), two or more resistance and two or more switching circuits are prepared. The resistance change circuit which has two or more current paths in which resistance changes mutually with combination of said resistance and switching circuit between said output stage driver component and said output terminal, said 1st reference potential terminal, or said 2nd reference potential terminal is constituted. The 1st semiconductor integrated circuit equipment with which it

comes to prepare the control terminal for a resistance change into which the signal which is connected to said each switching circuit, and controls a switching circuit is inputted, The process which prepares two or more 2nd semiconductor integrated circuit equipments electrically connected to said 1st semiconductor integrated circuit equipment through wiring of said mounting substrate, The process which carries said 1st semiconductor integrated circuit equipment and the 2nd semiconductor integrated circuit equipment in said mounting substrate, It judges based on the property of said mounting substrate or the 2nd semiconductor integrated circuit equipment. The control terminal for a resistance change of said 1st semiconductor integrated circuit equipment to the 1st reference potential wiring (power-source wiring) or the 2nd reference potential wiring (grand wiring) of said mounting substrate by the electrical connecting means It has the process to connect. Branching wiring for performing electrical installation with said control terminal for a resistance change is prepared in the 1st reference potential wiring (power-source wiring) or the 2nd reference potential wiring (grand wiring) of said mounting substrate, and said control terminal for a resistance change is electrically connected to said one of branching wiring. Said 1st semiconductor integrated circuit equipment is a driver IC, said 2nd semiconductor integrated circuit equipment is Memory IC, and the memory module is constituted on the whole.

[0019] According to the above (1), since the resistance change circuit which two or more control terminals for a resistance change are prepared in the driver IC, and was established in the interior by the signal impressed to these control terminals for a resistance change can be chosen, selection of an output impedance is attained.

[0020] According to the above (2), in case a driver IC is mounted in (a) mounting substrate, two or more control terminals for a resistance change and the reference potential terminal (the power supply terminal and grand terminal) of a mounting substrate which were prepared in the driver IC can be electrically connected so that adjustment with the input impedance of other semiconductor integrated circuit equipments (memory IC) electrically connected to a wiring impedance or said driver IC may suit. Consequently, it becomes, without the memory IC which an impedance mismatch stops having occurred, and the wave-like distortion of a driver IC also stops having also occurred, and was connected between a driver IC and Memory IC malfunctioning. Therefore, the memory module which can deliver a signal good can be offered.

[0021] (b) Impedance matching is connection actuation of the control terminal for a resistance change at the time of mounting of a driver IC, ends, by what is considered as the structure of preparing the control terminal for a resistance change beforehand, is not accompanied by modification of the circuit pattern in the middle in manufacture of a driver IC, i.e., modification of a photo mask etc., like before, but can attain reduction of the manufacturing cost of a driver IC.

[0022] (c) In a board manufacturer, the board (mounting substrate) which can perform impedance matching between driver ICs easily can be cheaply offered to a user that what is necessary is just to manufacture the mounting substrate which has the circuit pattern which can perform connection actuation with the control terminal for a resistance change.

[0023]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. In addition, in the complete diagram for explaining the gestalt of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.

[0024] (Operation gestalt 1) The circuit diagram showing some semiconductor integrated circuit equipments (driver IC) whose drawing 1 is 1 operation gestalt (operation gestalt 1) of this invention, and drawing 2 are the top views showing a driver IC.

[0025] The driver IC 4 is making two or more leads 8 project, respectively from the both-sides side of the package 7 which consists of a ** length rectangle object, as shown in drawing 2 . These-seven leads 8 are made to project from the both sides of a package 7 with this operation gestalt 1, respectively. the number given to the front face of a package 7 -- a lead terminal number -- it is -- 1 -- the 2nd reference potential terminal (gland: GND) and 2 -- for Input a - Input d, 8, or 11, as for a clock output (CLK output) and 13, an output d - an output a, and 12 are [the control terminal b for a resistance change

(control), and 3 / the control terminal a for a resistance change (control), 4, or 7 / clocked into (CLK) and 14] the 1st reference potential terminals (power supply terminal: Vcc).
[0026] In the output stage circuit of said driver IC 4, the resistance change circuit as shown in drawing 1 is prepared. This resistance change circuit is constituted by two or more resistance and two or more switching circuits. With this operation gestalt 1, resistance is prepared with Ra, Rb, and three Rc(s), and two switching circuits are prepared with 30a and 30b.
[0027] That is, in order to adjust the output impedance of a driver IC 4 during the wiring 18 between the output terminals 17 of the output stage driver component 10 constituted by N-channel metal oxide semiconductor FET11 and P channel MOSFET12, it has composition which has arranged Resistance Ra, Rb, and Rc to the serial.
[0028] Switching circuits 30a and 30b become the respectively same configuration, and consist of inverters 31a and 31b, N-channel metal oxide semiconductor FET 32a and 32b, and P channel MOSFETs 33a and 33b. The drain electrodes and source electrodes are connected, respectively, and the Nodes 34a and 34b and Nodes 35a and 35b are connected to the nodes 36a, 36b, and 36c of the input side of each resistance Ra, Rb, and Rc for N-channel metal oxide semiconductor FET 32a and 32b and P channel MOSFETs 33a and 33b through Wiring 37a, 37b, and 37c.
[0029] The control terminal a for a resistance change of lead 8 (control) is connected to the gate electrode of N-channel metal oxide semiconductor FET32a through inverter 31a while connecting with the gate electrode of P channel MOSFET33a through wiring 38a. Similarly, the control terminal b for a resistance change of lead 8 (control) is connected to the gate electrode of N-channel metal oxide semiconductor FET32b through inverter 31b while connecting with the gate electrode of P channel MOSFET33b through wiring 38b.
[0030] Thereby, the resistance of an output part when the "LOW" signal goes into the control terminals a and b for a resistance change becomes the sum total of the resistance of Resistance Ra, Rb, and Rc. Moreover, resistance when the "LOW" signal goes into the control terminal a for a resistance change (control) at the "HIGH" signal and the control terminal b for a resistance change (control) becomes the sum of the resistance of Resistance Rb and Rc. Moreover, resistance when the "HIGH" signal goes into the control terminal b for a resistance change (control) becomes only Resistance Rc.
[0031] Thus, switching circuits 30a and 30b operate, between the output node 14 of the output stage driver component 10, and an output terminal 17, a current path different, respectively will be formed of the electrical potential difference impressed to the control terminals a and b for a resistance change (control), and selection adjustment of the output impedance of a driver IC 4 will be made with it. By the number of the resistance prepared between the output node 14 and an output terminal 17, or selection of the resistance, resistance can be set up freely and can set up an impedance finely.
[0032] Drawing 3 is drawing showing the memory module (electronic instrument) 1 which included two memory (semiconductor integrated circuit equipment) IC 3 in the mounting substrate (board: memory module substrate) 2 with the driver IC 4 of this operation gestalt 1. The wiring 5 of a predetermined pattern is formed in the front face of a board 2. Moreover, the terminal 6 is formed in one side of a board 2. A clock terminal (CLK), the 1st reference potential terminal (power supply terminal: Vcc), the 2nd reference potential terminal (gland: GND), Vcc, Input a - Input d were located in a line one by one towards the right from the left, and many memory section input/output terminals are located in a line after that. The branching wiring 40a and 40b is formed in the 1st reference potential wiring (power supply terminal: Vcc) and the 2nd reference potential wiring (gland: GND), and electrical installation with said control terminals a and b for a resistance change (control) is performed. Electrical installation is connected with the conductive wires 41a and 41b with this operation gestalt 1. Such a memory module 1 prepares a board 2, memory IC 3, and a driver IC 4 first in the manufacture.
[0033] Next, as shown in drawing 4 , a driver IC 4 is carried in a board 2. The lead 8 of a driver IC 4 is electrically connected to wiring 5 by solder etc. Memory IC 3 is carried similarly.
[0034] Next, as shown in drawing 5 , the control terminals a and b for a resistance change of a driver IC 4 are connected to the 1st reference potential terminal (power supply terminal: Vcc) or the 2nd reference potential terminal (gland: GND) with Wires 41a and 41b. This connection is chosen by the quality of the

material and the wire length of a board 2, and among the resistance Ra, Rb, and Rc shown in drawing 1 , it chooses predetermined resistance and let [from] it be predetermined resistance. In this example, the control terminal a for a resistance change is connected to branching wiring 40b of grand wiring in wiring 5, and the control terminal b for a resistance change is connected to branching wiring 40a of power-source wiring in wiring 5. Consequently, the resistance of the output terminal 17 of a driver IC 4 is set to Rc.

[0035] According to this operation gestalt 1, it has the following effectiveness.

(1) In a driver IC 4, since the resistance change circuit which two or more control terminals a and b for a resistance change are formed, and was established in the interior by the signal impressed to these control terminals a and b for a resistance change can be chosen, selection of an output impedance is attained.

[0036] (2) In the memory module 1 which carried memory IC 3 and a driver IC 4 in the board 2, after mounting memory IC 3 and a driver IC 4 in a board 2, the quality of the material and the wire length of a board 2 are checked, and selection adjustment of the output impedance of a driver IC 4 can be performed. That is, adjustment of the impedance between a driver IC 4 and memory IC 3 is aimed at by connecting the control terminals a and b for a resistance change of a driver IC 4 to the branching wiring 40a and 40b of power-source wiring and grand wiring in wiring 5 through Wires 41a and 41b according to the quality of the material and the wire length of said board 2. It becomes without the memory IC 3 which an impedance mismatch stops having occurred, and the wave-like distortion of a driver IC 4 also stops having also occurred, and was connected between a driver IC 4 and memory IC 3 by this malfunctioning. Therefore, the memory module 1 which can deliver a signal good can be offered.

[0037] (3) Impedance matching is connection actuation of the control terminal for a resistance change at the time of mounting of a driver IC 4, ends, by what is considered as the structure of preparing the control terminal for a resistance change beforehand, is not accompanied by modification of the circuit pattern in the middle in manufacture of a driver IC, i.e., modification of a photo mask etc., like before, but can attain reduction of the manufacturing cost of a driver IC.

[0038] (5) In a board manufacturer, the board which can perform impedance matching between driver ICs easily can be cheaply offered to a user that what is necessary is just to manufacture the board (mounting substrate) 2 which has the circuit pattern which can perform connection actuation with the control terminal for a resistance change.

[0039] (Operation gestalt 2) Drawing 6 is the top view showing some memory module substrates which are other operation gestalten (operation gestalt 2) of this invention. With this operation gestalt 2, two control terminals a and b for a resistance change of a driver IC 4 are connected to branching wiring 40b of grand wiring in wiring 5 by each through Wires 41a and 41b, and as shown in drawing 1 , the resistance in the output terminal 17 of a driver IC 4 turns into a value of the sum total of Resistance Ra, Rb, and Rc.

[0040] Although invention made by this invention person above was concretely explained based on the operation gestalt It cannot be overemphasized that it can change variously in the range which this invention is not limited to the above-mentioned operation gestalt, and does not deviate from the summary, for example, although the resistance change circuit was prepared between the output stage driver component and the output terminal with said operation gestalt 1 Even if it prepares between an output stage driver component, the 1st reference potential terminal (power supply terminal), or the 2nd reference potential terminal (grand terminal), selection adjustment of the output impedance of a driver IC can be attained like said example.

[0041] Although the above explanation explained the case where invention mainly made by this invention person was applied to the manufacturing technology of the memory module which is a field of the invention used as the background, it is not limited to it and can apply to the manufacturing technology of other electronic instruments etc.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram showing some semiconductor integrated circuit equipments which are 1 operation gestalt (operation gestalt 1) of this invention.
[Drawing 2] It is the top view showing the semiconductor integrated circuit equipment of this operation gestalt 1.
[Drawing 3] It is the top view showing the memory module (electronic instrument) carrying the semiconductor integrated circuit equipment of this operation gestalt 1.
[Drawing 4] They are some top views showing the condition of having carried the semiconductor integrated circuit equipment of this operation gestalt 1 in the memory module substrate in manufacture of said memory module.
[Drawing 5] It is the top view showing some memory module substrates with which impedance adjustment of the output stage circuit of semiconductor integrated circuit equipment was made in manufacture of said memory module.
[Drawing 6] It is the top view showing some memory module substrates which are other operation gestalten (operation gestalt 2) of this invention.
[Drawing 7] It is the mimetic diagram showing the conventional memory module.
[Drawing 8] It is a circuit diagram by the conventional technique which prepared series resistance in the output stage circuit of semiconductor integrated circuit equipment.
[Drawing 9] It is the wave form chart showing an example of the waveform distortion generated by the mismatching of the impedance of wiring connected with semiconductor integrated circuit equipment at this, or other semiconductor devices.
[Description of Notations]
1 -- A memory module, 2 -- Mounting substrate (a board 1, memory module substrate), 3 [-- A terminal, 7 / -- Package,] -- Memory IC, 4 -- A driver IC, 5 -- Wiring, 6 8 -- A lead, 10 -- An output stage driver component, 11 -- N-channel metal oxide semiconductor FET, 12 -- P channel MOSFET, 13 -- An input node, 14 -- Output node, 15 [-- Wiring,] -- A power supply terminal, 16 -- A GND terminal, 17 -- An output terminal, 18 19 [-- Switching circuit,] -- Resistance, 20 -- The wave, 21 which should be expected -- A wave, 30a, 30b which distortion generated 31a, 31b -- An inverter, 32a, 32b -- N-channel metal oxide semiconductor FET, 33a, 33b [-- Branching wiring 41a, 41b / -- Wire.] -- P channel MOSFET, 34a, 34b, 35a, 35b, 36a, 36b, 36c -- A node, 37a, 37b, 37c, 38a, 38b -- Wiring, 40a, 40b

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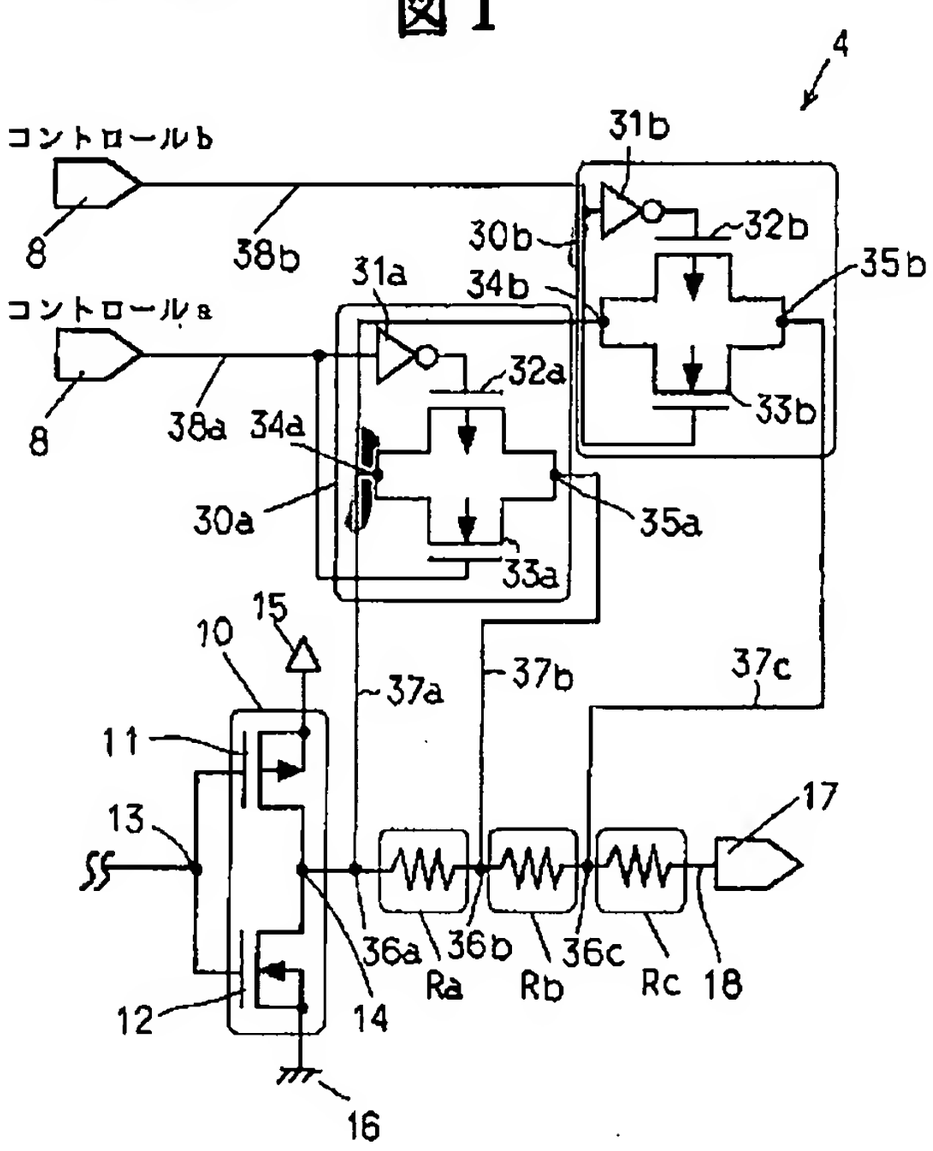
DRAWINGS

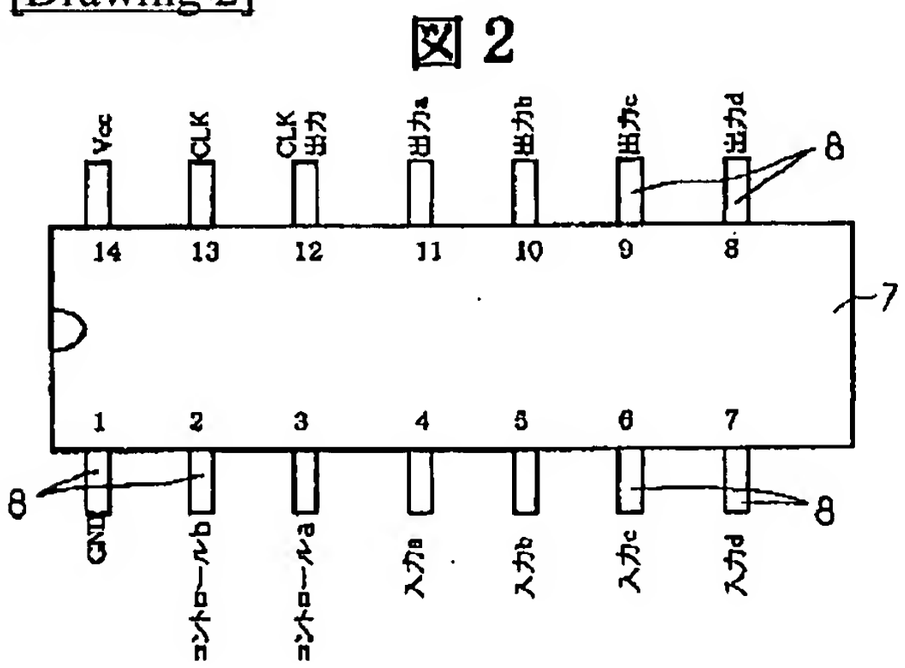
[Drawing 1]

図 1



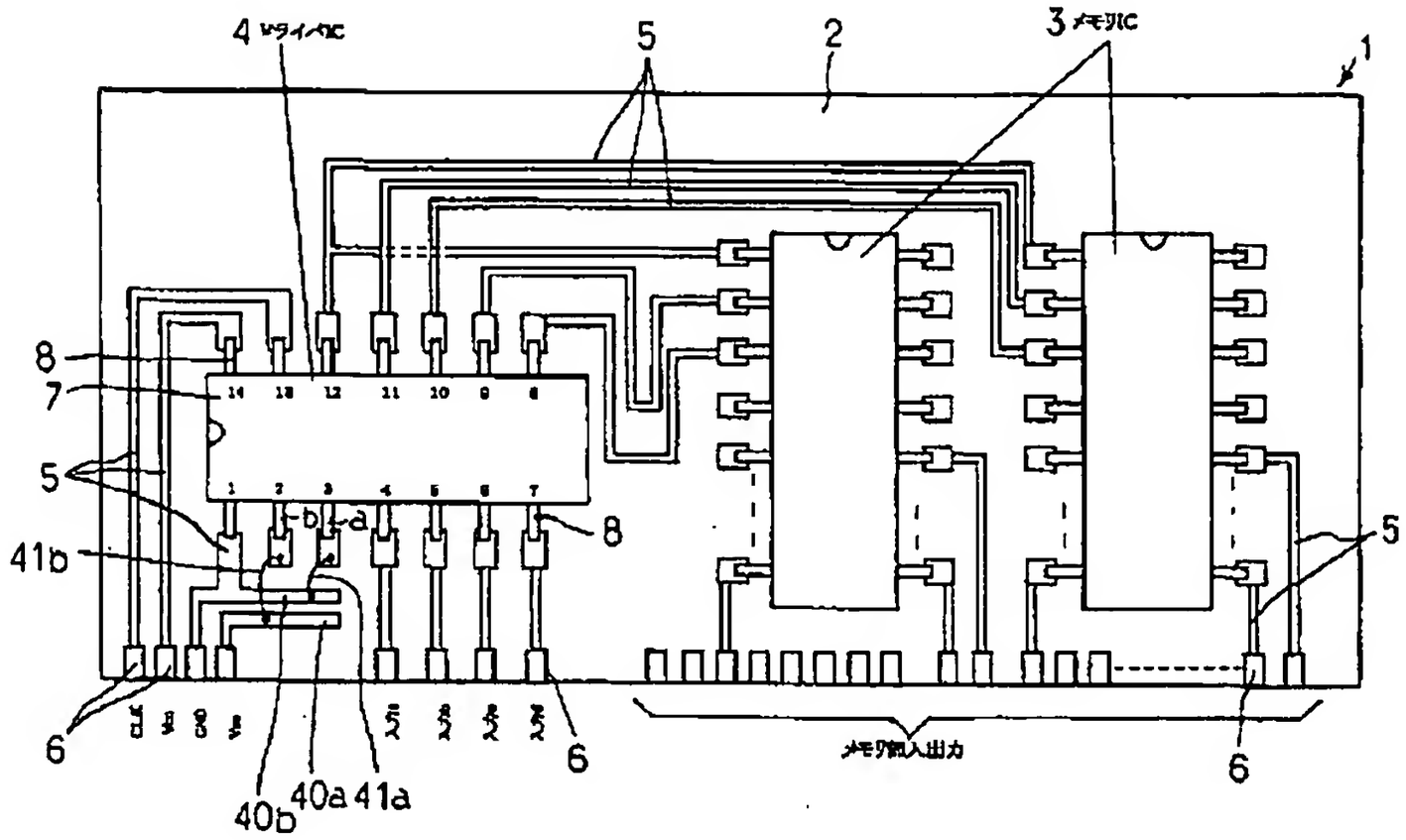
[Drawing 2]

図 2



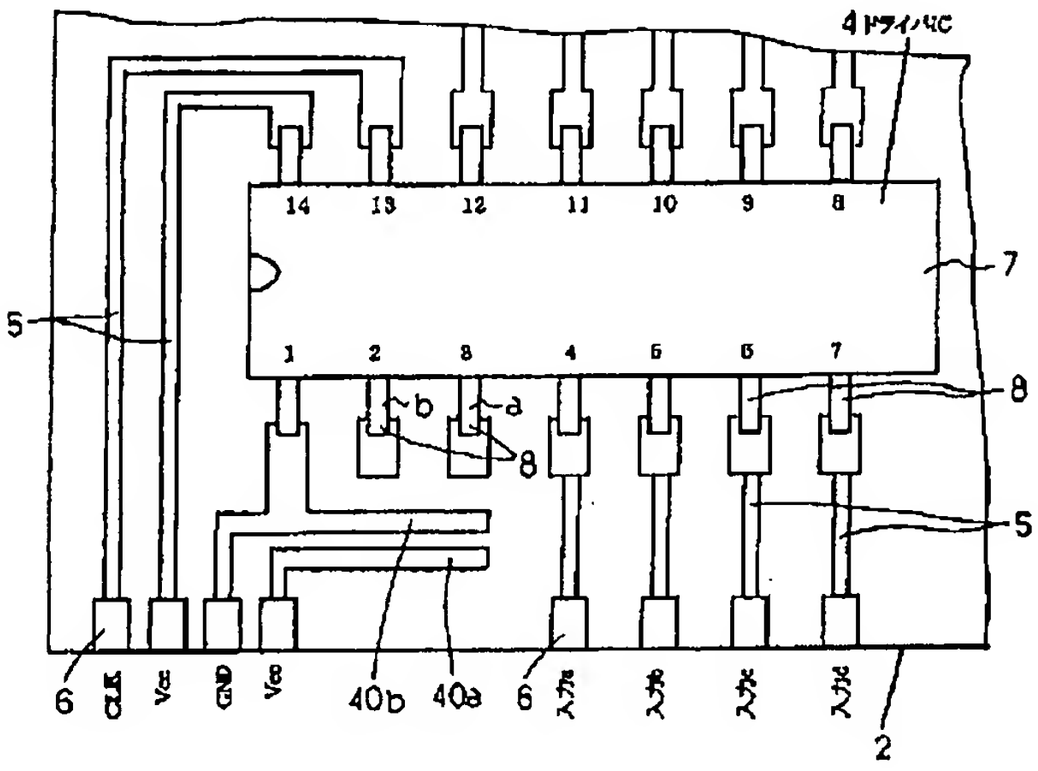
[Drawing 3]

図 3



[Drawing 4]

図 4



[Drawing 5]

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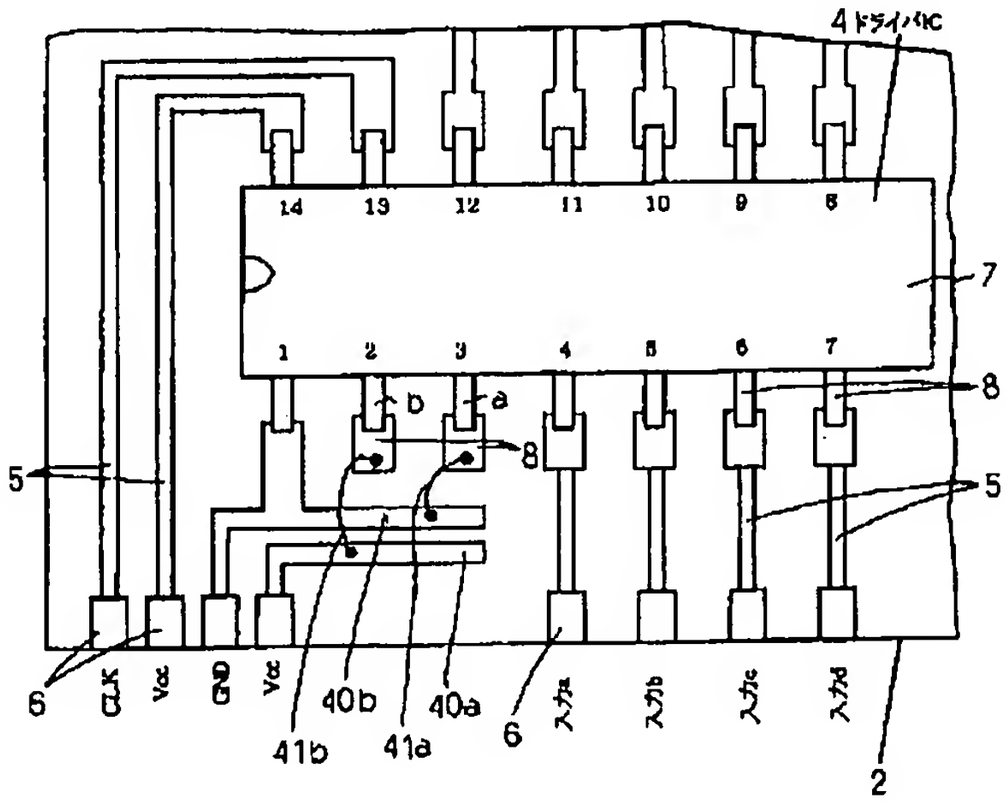
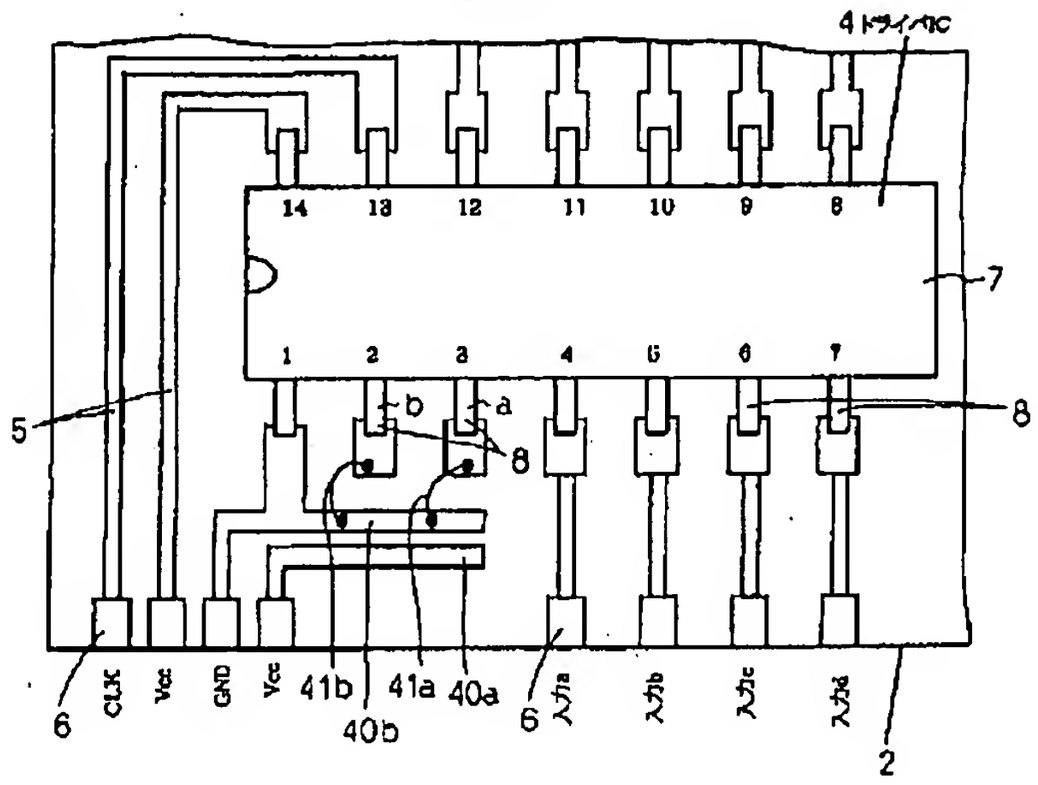


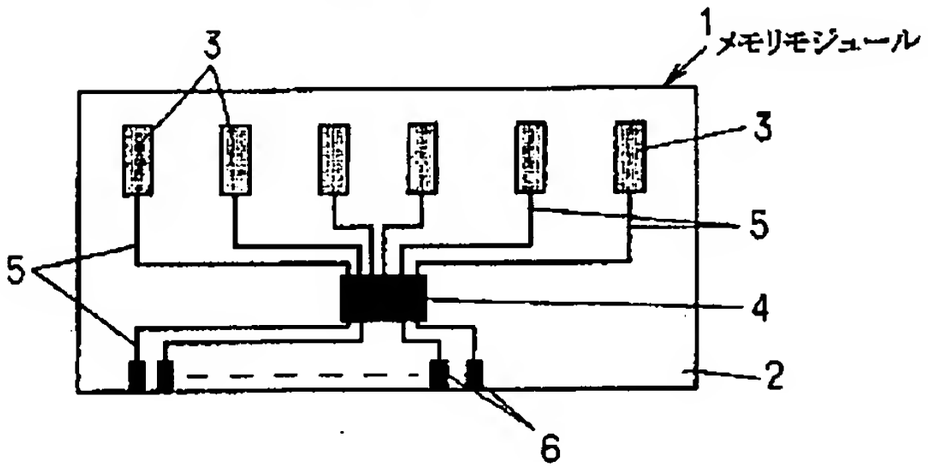
[Drawing 6]

図 6



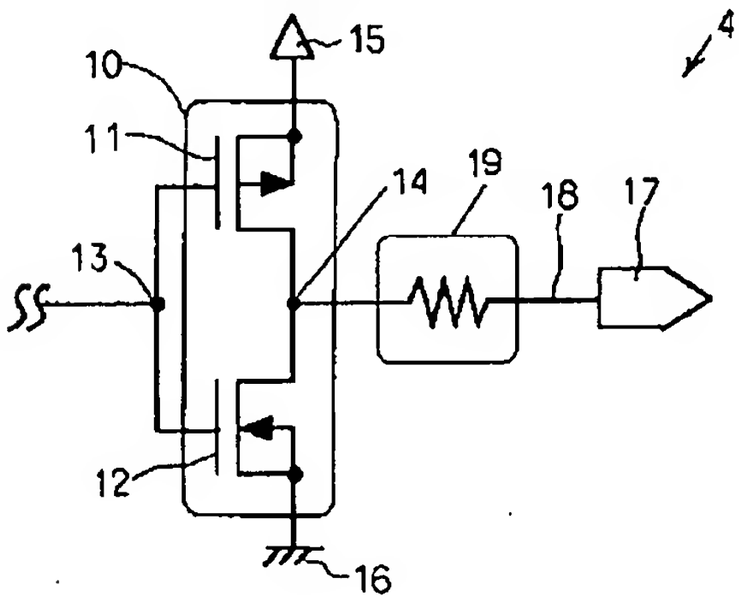
[Drawing 7]

図 7



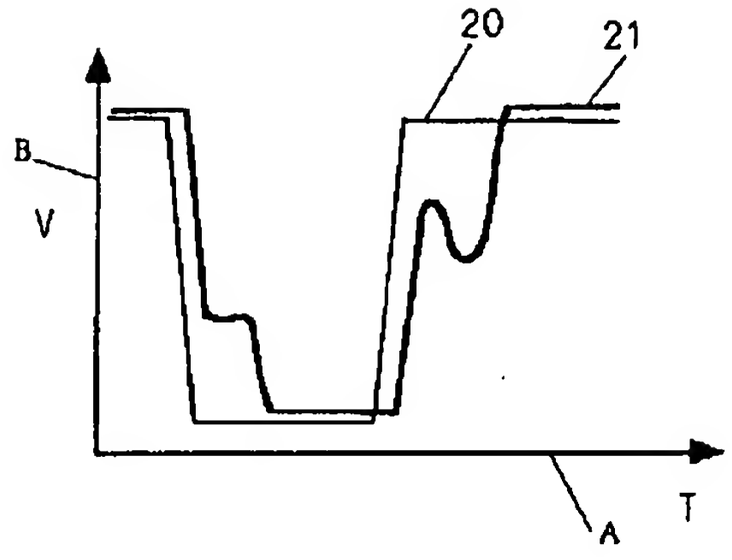
[Drawing 8]

図 8



[Drawing 9]

図 9



[Translation done.]